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Fig. 1

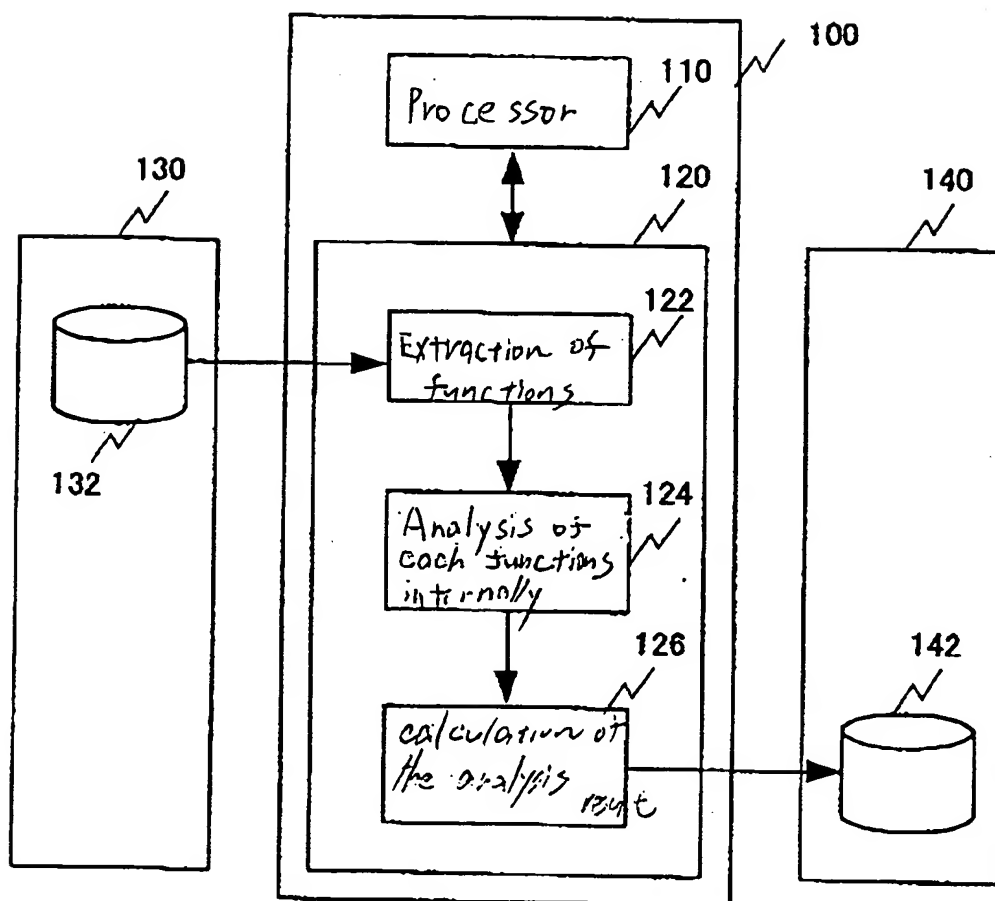


Fig. 2

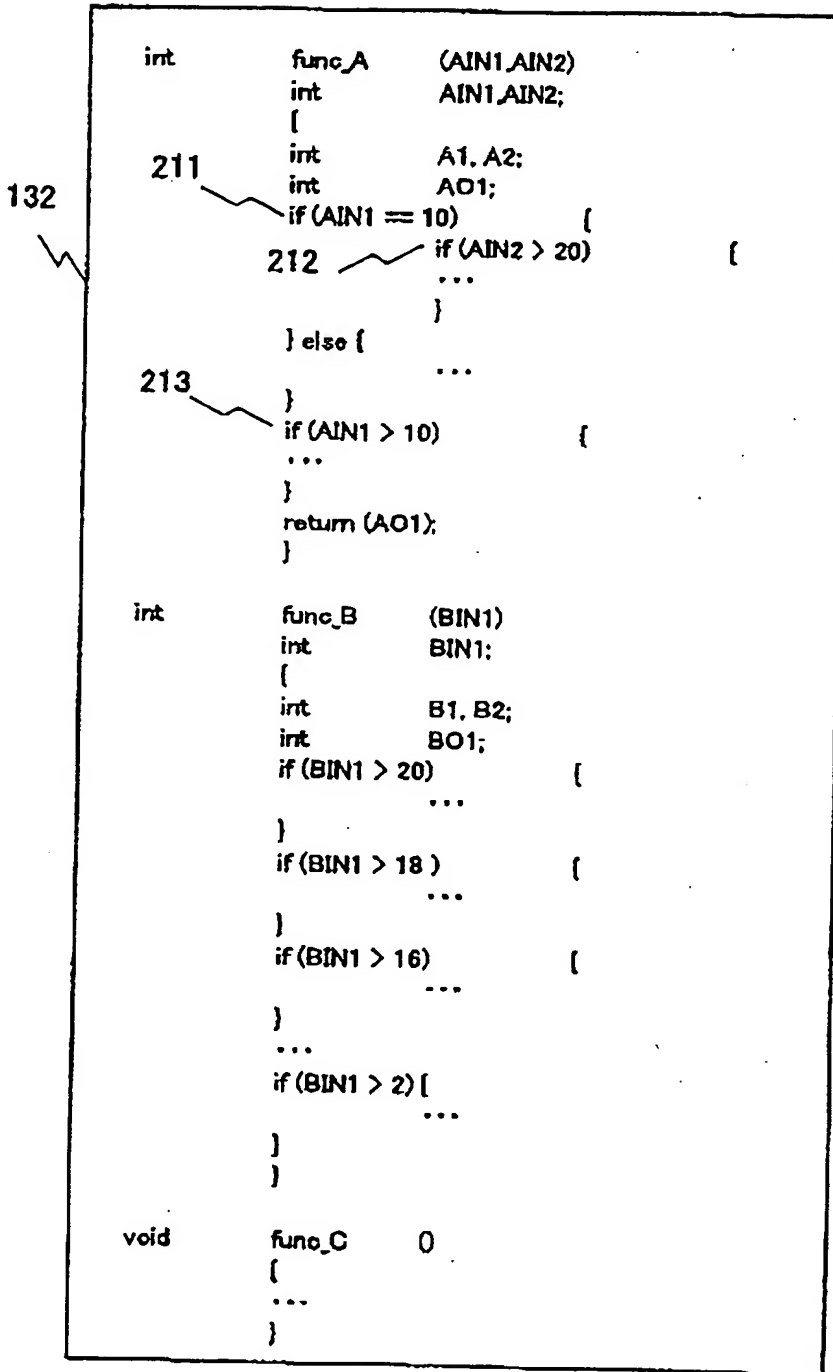


Fig. 3

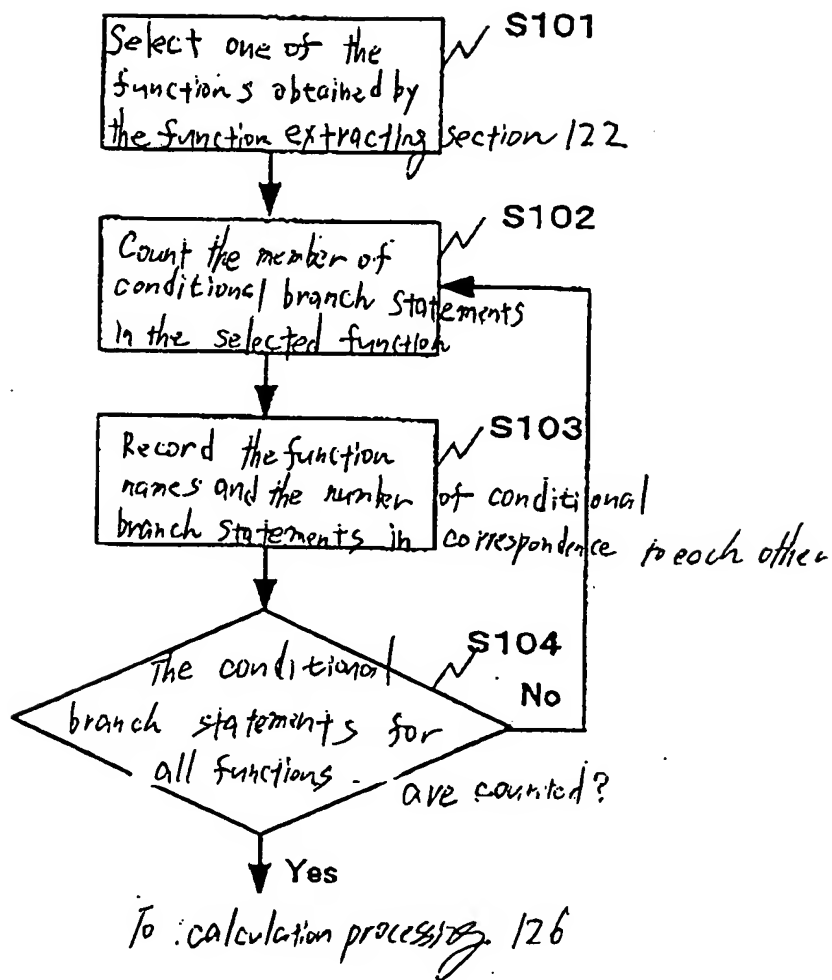


Fig. 4

Function name	Number of conditional branch statements
func_A	3
func_B	10
func_C	0

Fig. 5

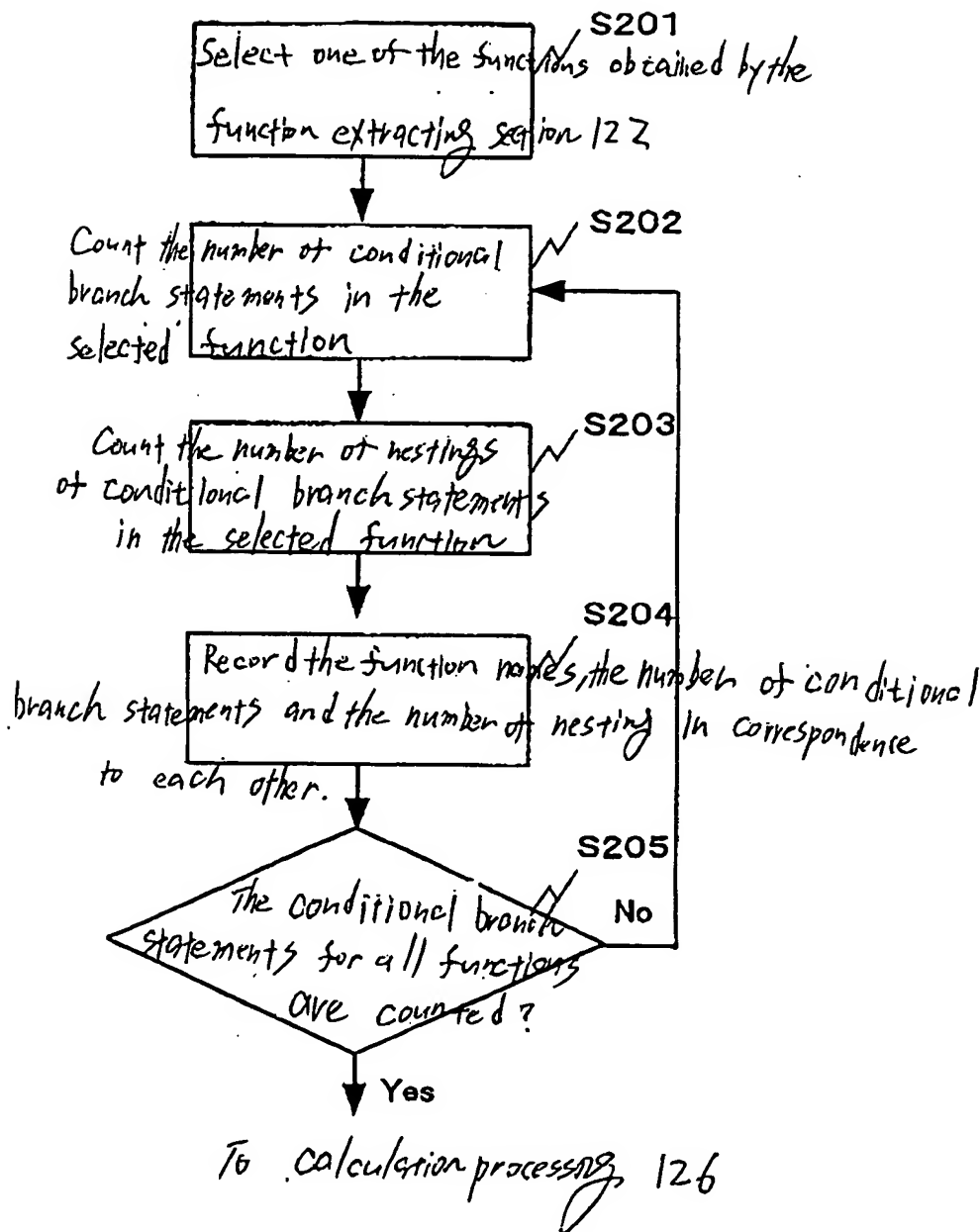


Fig. 6

Function name	Conditional branch statement		
	Number	Number of nestings	
		Number of nesting starts	Number of corresponding conditional branch statements
func_A	3	0	2
		1	1
func_B	10	0	10
func_C	0	0	0

conditional branch statements

Fig. 7

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```

int func_A (AIN1, AIN2)
{
    int A1, A2;
    int AO1;
    211 if (AIN1 == 10) {
        212 if (AIN2 > 20) {
            ...
        }
        } else {
            ...
        }
    213 }
    if (AIN1 > 10) {
        ...
    }
    return (AO1);
}

void func_D ()
{
    int D1, D2, D3;
    711 D2 = func_A1 ( D1 );
    712 AIN1 = func_A2 ( D2 );
    ...
    D3 = func_A ( AIN1, D2 );
}

```

Fig. 8

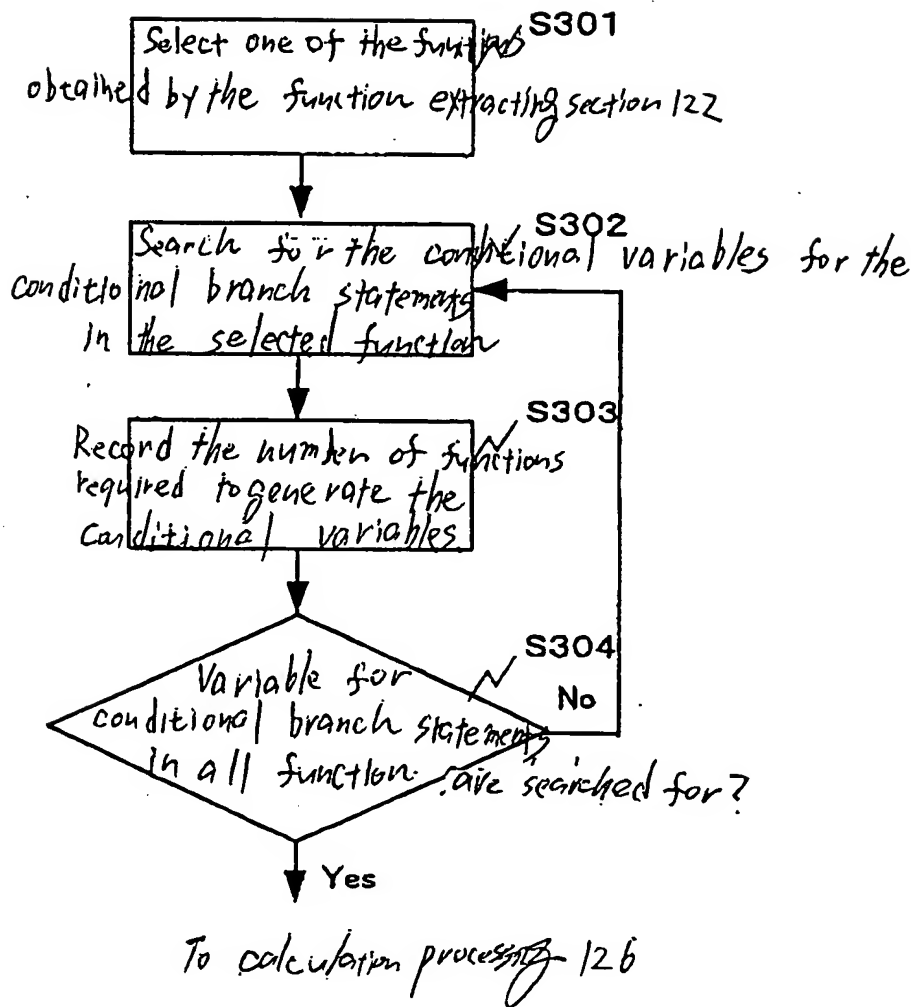


Fig. 9

Function name	Conditional branch statement		
	Number	Variable generation	
		Number of functions required for generation	Number of variables
func_A	3	2	1
		0	1
func_D	0	0	0

Fig. 10

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```

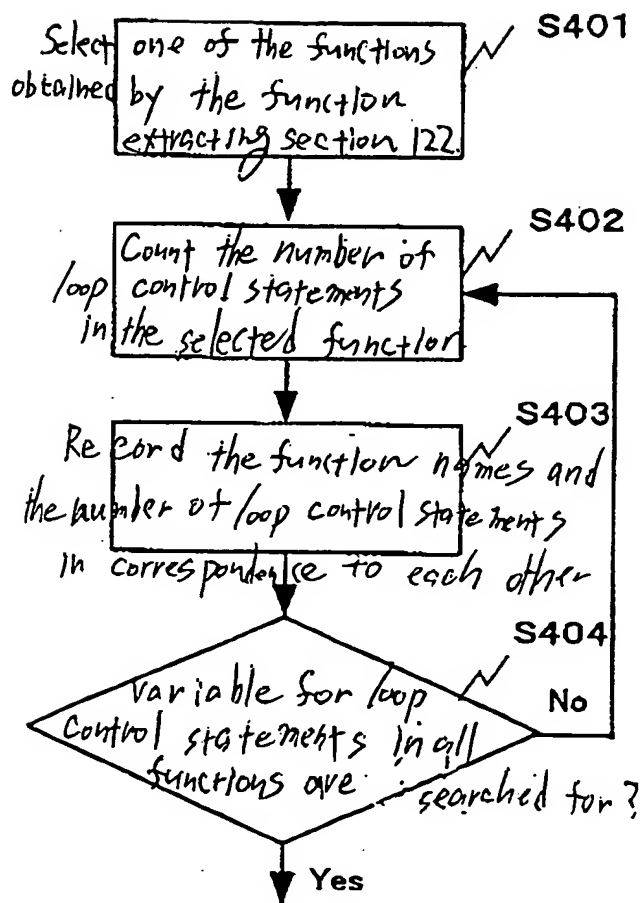
int      func_LA      (AIN1,AIN2)
int
{
  int      ij;
  int      A1, A2;
  int      AO1;
  for (i = 0; i < AIN1; ++i) {
    for (j = 0; j < AIN2; ++j) {
      ...
    }
    ...
  }
  for (i = 0; i < 10; ++i) {
    ...
  }
  return (AO1);
}

int      func_LB      (BIN1)
int
{
  int      i;
  int      B1, B2;
  int      BO1;
  for (i = 0; i < BIN1; ++i) {
    ...
  }
  for (i = 0; i < BIN1; ++i) {
    ...
  }
  for (i = 0; i < BIN1; ++i) {
    ...
  }
  ...
  for (i = 0; i < BIN1; ++i) {
    ...
  }
  ...
}

void     func_LC      0
{
  ...
}

```


Fig. 11



To calculation processing 126

Fig. 12

Function name	Number of loop control statements
func_LA	3
func_LB	10
func_LC	0

Fig. 13

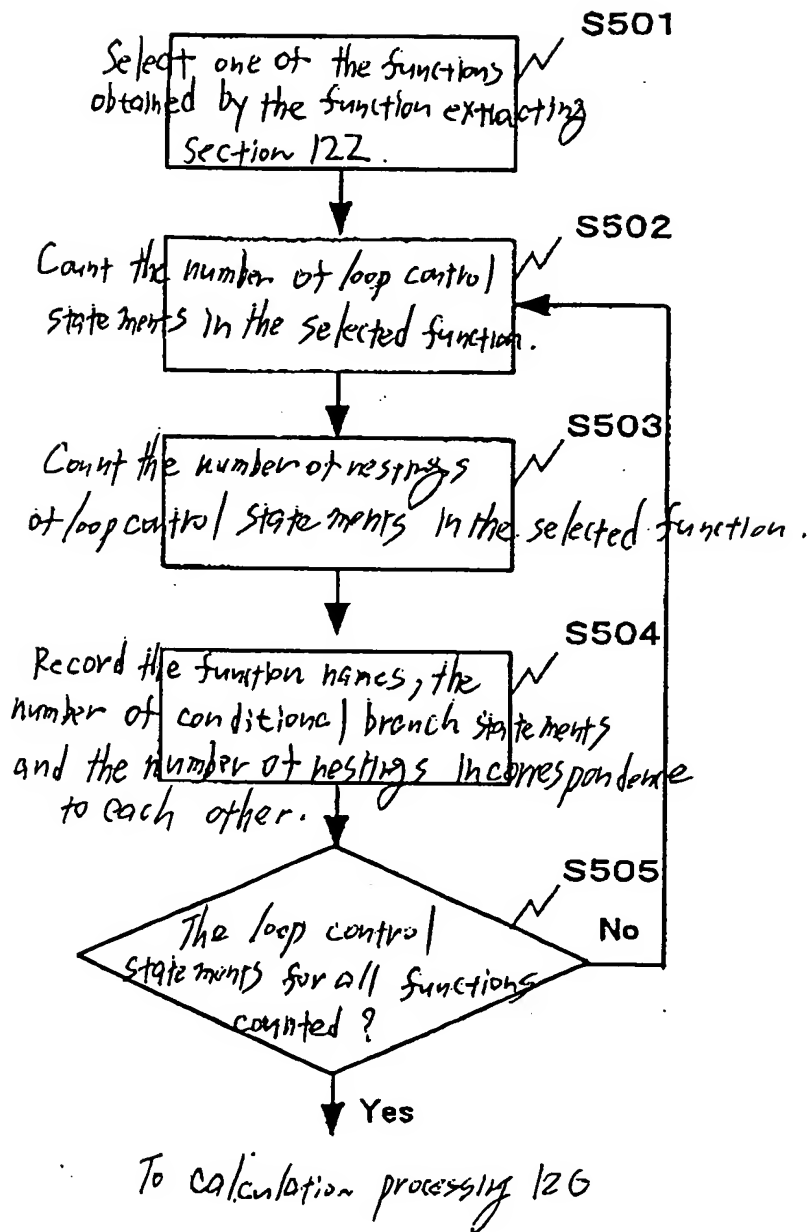


Fig. 14

Function name	Loop control statement		
	Number	Number of nesting	
		Number of nesting steps	Number of corresponding loop control statements
func_LA	3	0	2
		1	1
func_LB	10	0	10
func_LC	0	0	0

Fig. 15

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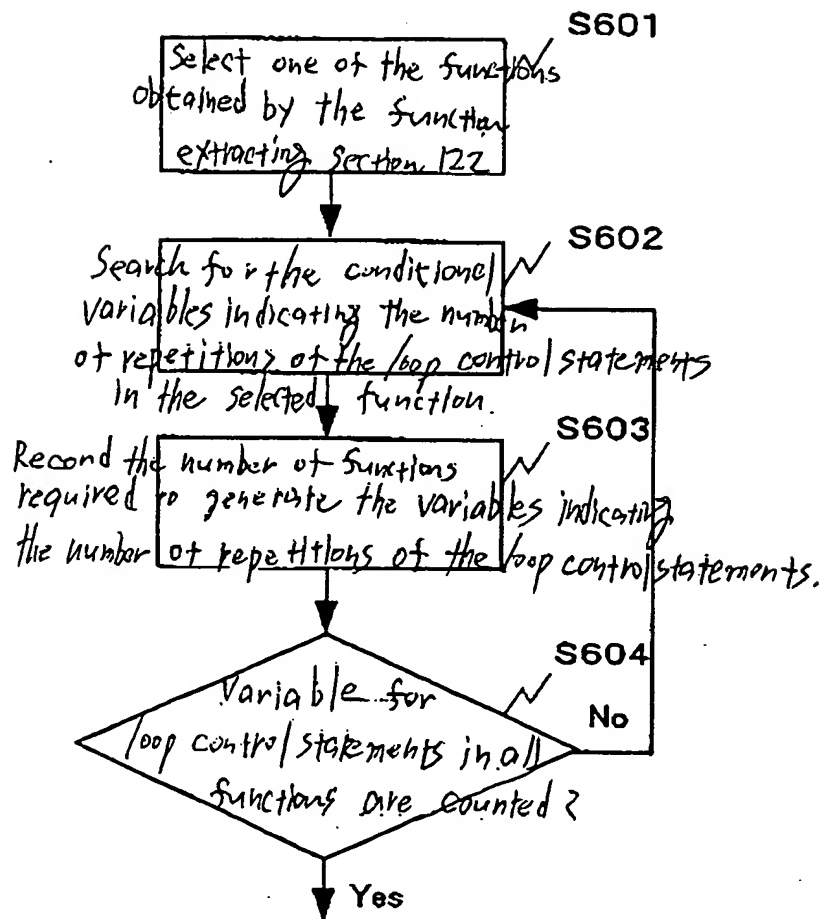
```

int      func_LA  (AIN1, AIN2)
int      AIN1, AIN2;
{
1011    int      A1, A2;
1012    int      AO1;
        for (i = 0; i < AIN1; ++i) {
            for (j = 0; j < AIN2; ++j) {
                ...
            }
            ...
        }
1013    for (i = 0; i < 10; ++i) {
        ...
    }
    return (AO1);
}

void      func_LD  ()
{
1511    int      D1, D2, D3;
        D2 = func_LA1 ( D1 );
1512    AIN1 = func_LA2 ( D2 );
        ...
        D3 = func_LA ( AIN1, D2 );
}

```

Fig. 16

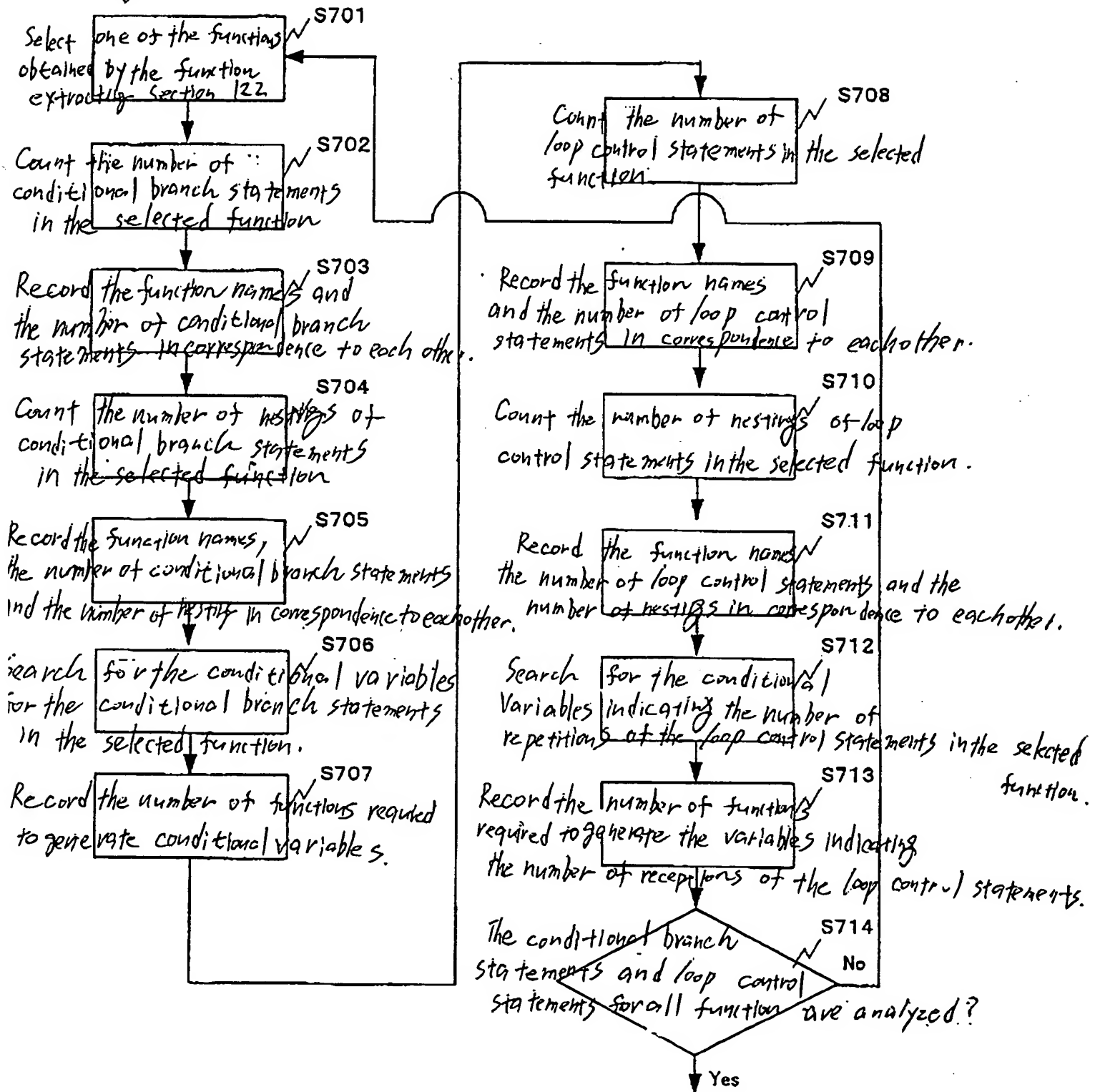


To calculation processing 126

Fig. 17

Function name	Loop control statement		
	Number	Variable generation for the number of repetitions	
		Number of functions required for generation	Number of variables
func_LA	3	2	1
		0	1
func_LD	0	0	0

Fig. 18



To calculation processing 126

Fig. 19

for the number of repetitions

conditional branch statements

Function name	Conditional branch statement			Loop control statement		
	Number	Number of nestings		Number	Number of nestings	
		Number of nesting stages	Variable generation		Number of nestings	Number of nestings
func_A	3	0	2	0	0	0
		1	1			
func_B	10	0	10	0	0	0
func_C	0	0	0	0	0	0
func_D	0	0	0	0	0	0
func_LA	0	0	0	3	2	1
func_LB	0	0	0	10	10	1
func_LC	0	0	0	0	0	0
func_LD	0	0	0	0	0	0

Number of functions required for generation

Fig. 20

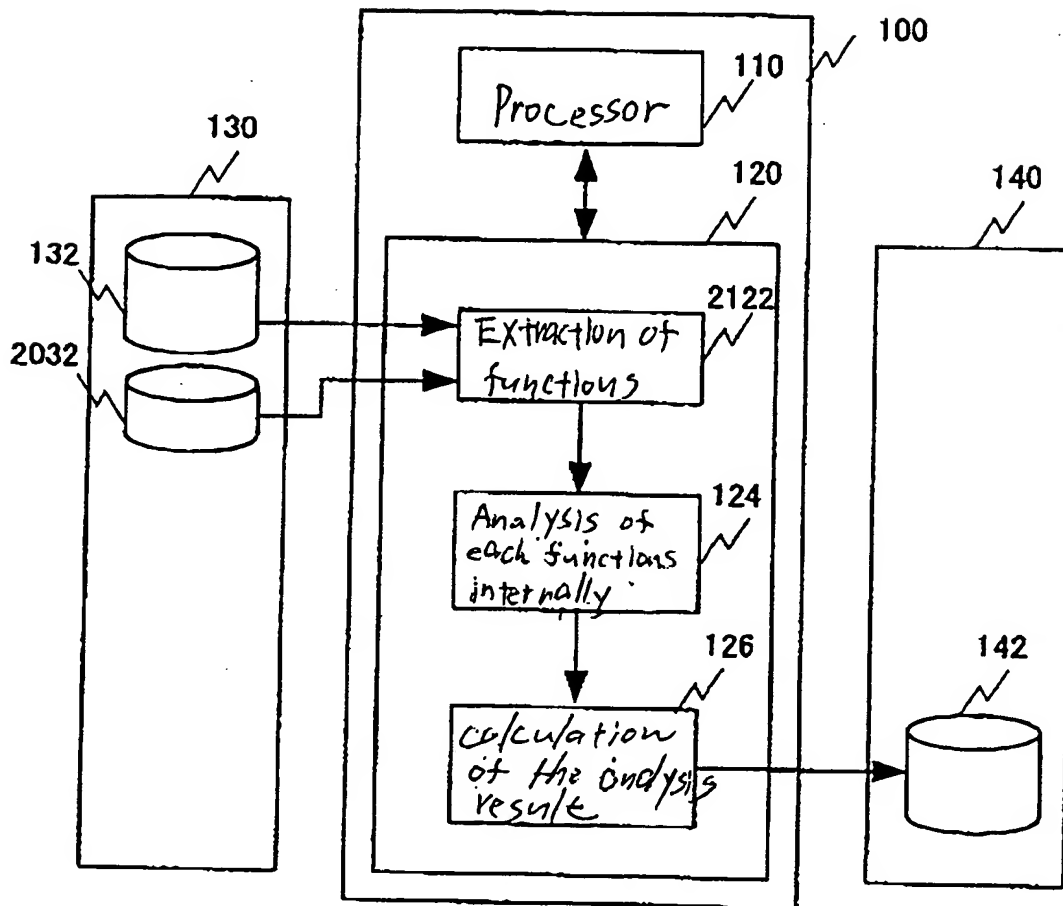


Fig. 21

Function name	Conditional branch statement		
	Number	Variable generation	
		Number of functions required for generation	Number of variables
func_A + func_D	3	2	1
		0	1

Fig. 22

Function name	Loop control / statement		
	Number	Generation of variables for the number of repetitions	
		Number of functions require for generation	Number of variables
func_LA + func_LD	3	2	1
		0	1

Fig. 23

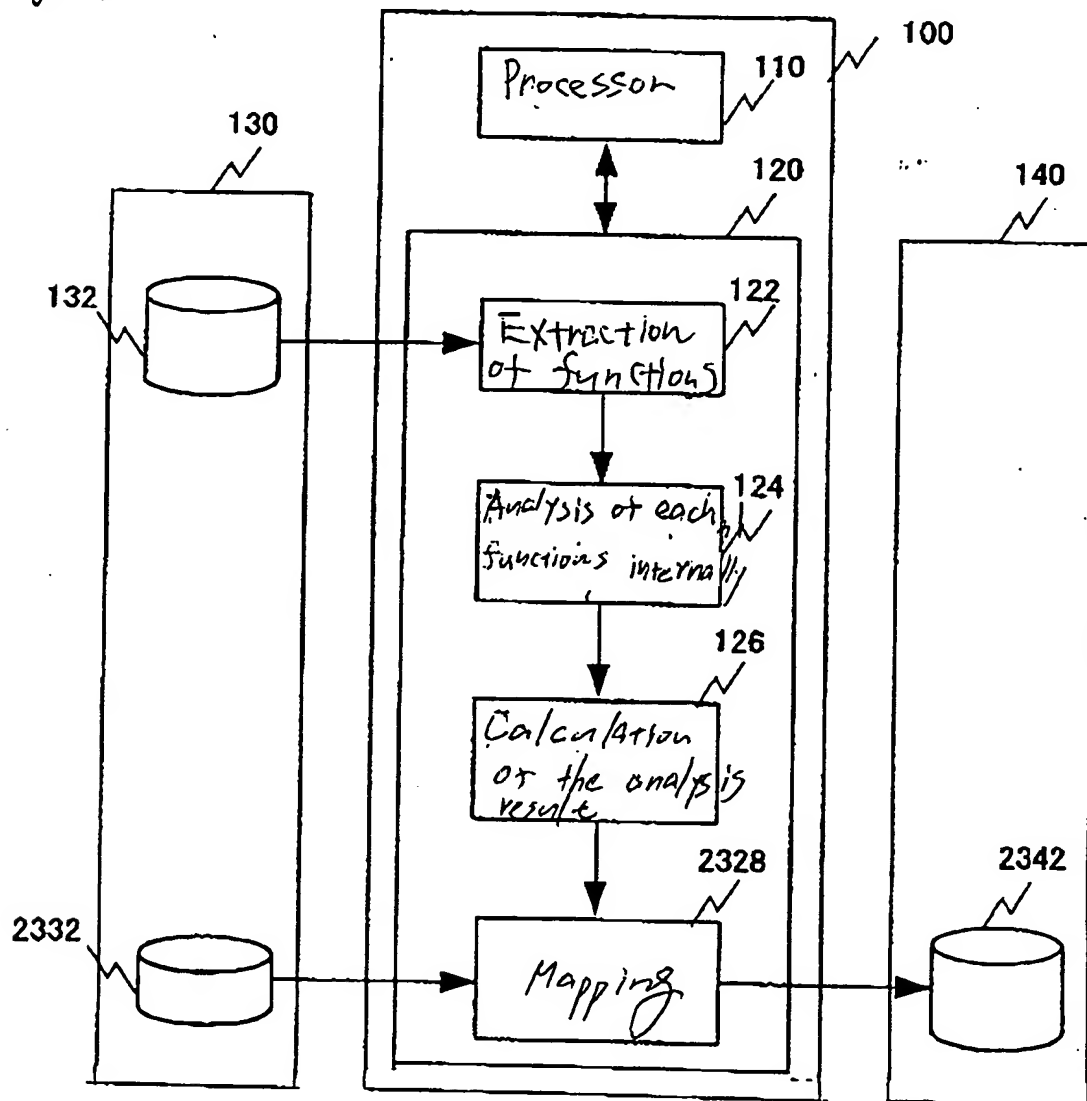


Fig. 24

Processing unit	Preferable Number of conditional branch statements
CPU	10 or more
DSP	3 to 9
Dedicated logic	2 or less

Fig. 25

Function name	Appropriate processing unit
func_A	DSP
func_B	CPU
func_C	Dedicated logic

Fig. 26

Processing unit	Preferable number of loop control statements
CPU	3 to 9
DSP	10 or more
Dedicated logic	2 or less

Fig. 27

Function name	Appropriate processing unit
func_LA	CPU
func_LB	DSP
func_LC	Dedicated logic

Fig. 28

Function name	Appropriate conditional branch statement					Appropriate loop control statement			
	number	Number of nestings		Variable generation		number	Number of nestings for number of repetition		
		Number of nestings	Number of corresponding conditional branch statements	Number of corresponding conditional branch statements	Number of variables		Number of corresponding control statements for generation	Number of functions required	Number of variables
OFU	10 or more	0	1 or more	0	1 or more	3 to 9	0	3 to 9	3 to 9
		1	1 or more	1	1 or more		1	0	1
		2 or more	1 or more	2 or more	1 or more		2 or more	0	2 or more
DSP	3 to 9	0	3 to 9	0	3 to 9	10 or more	0	1 or more	0
		1	3 or less	1	3 or less		1	1 or more	1
		2 or more	1 or less	2 or more	1 or less		2 or more	1 or more	2 or more
Re directed logic	2 or less	0	3 or less	0	3 or less	3 or less	0	3 or less	3 or less

Fig. 29

Function name	Appropriate condition / branch statement			Appropriate loop control statement		
	Number	Number of nestings		Number	Number of nestings	
		Number of nesting stages	Number of corresponding conditional branch statements		Number of corresponding loop control statements	Number of repetitions
CPU	10 or more (K=8)	0 (K=1)	1 or more (K=1)	3 to 9 (K=1)	0 (K=1)	3 to 9 (K=1)
		1 (K=2)	1 or more (K=2)	10 or more (K=6)	0 (K=1)	0 (K=1)
		2 or more (K=3)	1 or more (K=3)	10 or more (K=6)	0 (K=1)	0 (K=1)
DSP	3 to 9 (K=7)	0 (K=1)	3 to 9 (K=1)	10 or more (K=6)	0 (K=1)	2 or less (K=2)
		1 (K=2)	2 or less (K=2)	10 or more (K=6)	0 (K=1)	2 or less (K=2)
		2 or more (K=3)	2 or less (K=3)	10 or more (K=6)	0 (K=1)	2 or less (K=2)
Dedicated logic	K=6	0 (K=1)	3 or less (K=1)	3 or less (K=6)	0 (K=1)	3 or less (K=2)

$$\text{CPU} = 3 + 4 + 2 + 2 = 11$$

$$\text{DSP} = 6 + 4 + 4 + 6 = 20$$

$$\text{Dedicated logic} = 1 + 1 + 6 + 2 + 2 = 12$$

Fig.30

Function name	appropriate processing unit
func_A	DSP
func_B	CPU
func_C	Dedicated logic
func_LA	CPU
func_LB	DSP
func_LC	Dedicated logic